METHOD AND APPARATUS FOR SAVING POWER IN PIPELINED PROCESSORS

ABSTRACT OF THE DISCLOSURE

Techniques for reducing power consumption in pipelined processors are described. As a method, one embodiment of the present invention reduces power requirements in a piplelined processor by evaluating instructions to be executed to determine the operation type of the instructions, producing activity indicators based upon the operation types of the instructions, and controlling the supply of current to each of the stages such that only selected stages draw current from a power supply.